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COMPACT MODELING OF LOW-POWER AND RF ANALOGUE MOSFET DEVICES

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ABSTRACT

The technology of CMOS very large-scale integrated circuits (VLSI's) achieved remarkable advances over the last 25 years and the progress is expected to continue well into this century. The progress has been driven by the downsizing of the key devices: MOSFETs. Approaching these dimensions, MOSFET characteristics cannot be accurately predicted using classical modeling methods currently used in the most common MOSFET models such as BSIM3/4, EKV v2.6, HiMOS, MOS9 etc., without introducing large number of empirical parameters. Various physical effects that are needed to be considered while modeling UDSM devices: quantization of the inversion layer, mobility degradation, carrier velocity saturation and overshoot, polydepletion effects, bias dependent source/drain resistances and capacitances, vertical and lateral doping profiles, etc. In this paper, we will discuss the progress in CMOS technology and anticipated difficulties of the sub-0.25μm VLSI downsizing. Subsequently, basic MOSFET modeling methodologies that are more appropriate for low power and RF analogue applications of UDSM MOSFETs will be presented as well.