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ADIABATIC MEMORIES – A REVIEW

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ABSTRACT

Adiabatic Logic is a promising approach with respect to power optimization in digital circuit design. In the recent years researches are carried out to design low power memories using this concept. The various adiabatic memories proposed in the recent years are outlined in this paper.

1. Introduction

With more and more portable systems coming in to operation design for low power consumption becomes a very important criteria for the designers. At the various levels of design abstraction, a variety of techniques are used to reduce the overall power dissipation. Now as the conventional methods of power reduction reach their limits non-conventional methods like adiabatic logic promise a greater power reduction capabilities. The Adiabatic logic also known as Energy recovery logic works by restricting the current to flow across the devices with low voltage drop and recycling the energy stored on their capacitors [1]. A number of adiabatic logic families have been proposed.

Though a lot of work has been made on implementing the logic circuits only a handful of work has been made in designing adiabatic memories. This fact has one main reason namely low operating frequency. But this limit is slowly overcome with the design of high-speed adiabatic memories. In this paper the evolution and growth of the concept of adiabatic memory design is discussed in detail.

The first chapter deals with Static Random Access Memory (SRAM) design, the second chapter with register file and the third chapter with Content Addressable Memory (CAM).

2. Energy Recovery SRAM

The energy recovery SRAM [2] (Fig. 1) uses a memory cell identical in topology to the six transistors SRAM used in the standard SRAM. Unlike the standard SRAM core in which the V_{HI} and V_{LO} signals are static here the V_{HI}, V_{LO} and word are generated by word driver circuitry. The row selection signal sel and sel/ enable the drivers for a particular row. The V_{HI}, V_{LO} and word for the row is controlled independently by driving G_{HI}, G_{LO} and G_{word}, respectively. Also (Fig. 1) shows transmission gate to

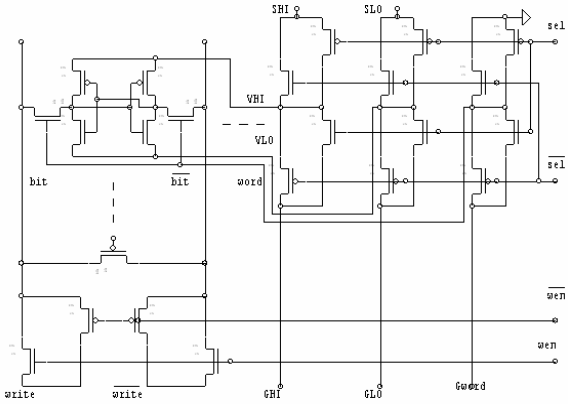

Fig. 1. Energy recovery SRAM core.

isolate write and write/ signals from bit and bit/ and a bit-line equalization transistor. By proper application of stimulus at V_{HI}, V_{LO}, word, bit and bit/ energy is recovered in a non-dissipative manner. The V_{HI} ranges from V_{CC} to $(V_{CC} + V_{keep})/2$ and V_{LO} ranges from $(V_{CC} - V_{keep})/2$ to 0 where V_{CC} is the supply voltage and V_{keep} is the minimum differential voltage across the cell to hold its state. In the read operation complete energy recovery is possible. But the write operation is not truly reversible. This energy recovery SRAM [2] shows energy savings of 84% for the read operations and 85% savings for the write operations.

Another energy recovery SRAM is given in [3]. The main difference between this and Conventional

SRAM is the latch and the driver. Memory cell is the conventional 6-T memory cell.

The energy recovery latch/driver is shown above (Fig. 2). It operates on bootstrapping effect and uses a two-phases power-clock. As a filter it either passes the clock pulses to the output or clamps the output to the ground depending on the stored datum. In addition as the latches drive the high-capacitance lines through nFETS the dissipation inside the latches is reduced and makes the overall size smaller. A 256x256 memory configuration of this energy recovery SRAM [3] with on average 50% of the bit lines switching in the successive write operations shows energy saving of 55% at 200 MHz operating frequency compared to the conventional design.

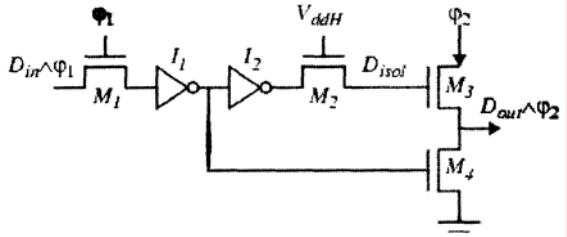

Fig. 2. Energy recovery latch/driver.

The energy recovery SRAM [4] (Fig. 3) also uses the conventional 6 T cell. It uses drivers which recovers energy from the capacitors of the bit/word lines. The driver has feedback path, which makes the energy recover efficiency independent of the operating frequency. To enable single-cycle reads with a single-phase power-clock, a precharge-low approach is used. A modified sense amplifier (Fig. 4) that operates efficiently at bit line voltages near V_{ss} is implemented. A 256x256 adiabatic SRAM that includes the energy recovery bit/word line drivers, the cell array and sense amplifiers shows 62% energy saving at 3 V, 300 MHz in comparison with its conventional counter part.

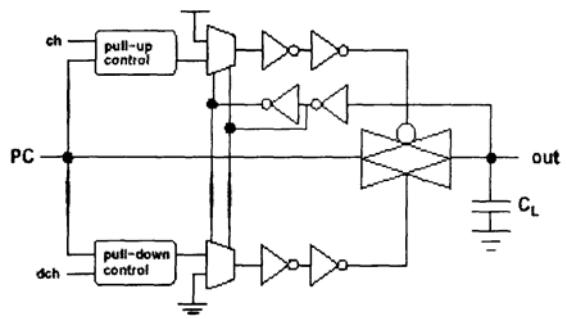

Fig. 3. Energy recovery driver with feedback.

Another low-complexity energy recovery SRAM with a single-phase power-clock is given in [5]. Memory load to power-clock during write is kept fixed by precharging non-selectively after each write cycle. Load during read is also kept fixed by not driving the bit lines with power-clock for read. A simple power-clock generator control scheme that exploits the fixed-load characteristics of the energy

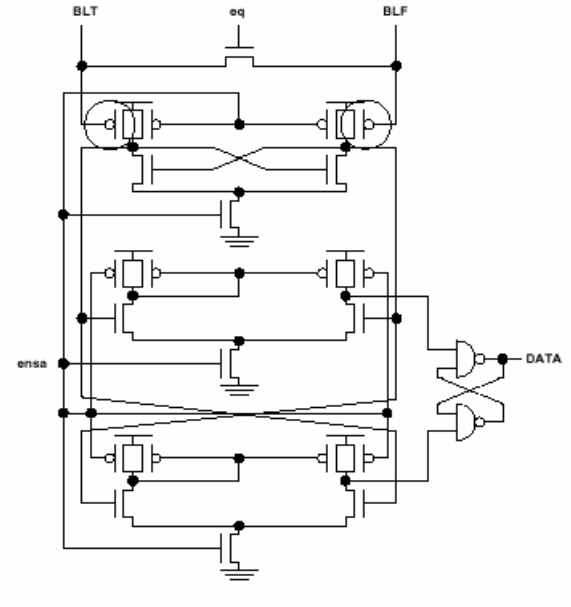

Fig. 4. Modified sense amplifier.

recovery memory is introduced to achieve substantially reduced total system power dissipation. The power-clock control scheme reduces the system dissipation by preventing the replenishing operation of the power-clock generator while not writing and thus does not require energy transfer between the memory and the power-clock. A full custom 128x256 energy recovery SRAM core [5] shows energy saving of 79% for the write operations in comparison with its conventional counterpart at 2.5 V, 250 MHz.

A constant load energy recovery SRAM design [6] provides a constant capacitive load to the power-clock, regardless of memory operation or data access pattern. Moreover non-selective precharge is used to ensure a constant memory load during the write operations, regardless of data pattern. Also when bit lines are disconnected from the power-clock during non-write cycles, dummy bit lines of equal capacitance are connected to the power-clock as shown (Fig. 5) containing a constant memory load.

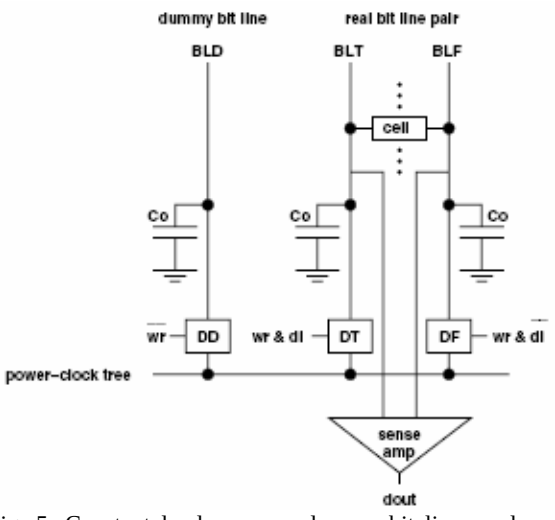

Fig. 5. Constant load memory dummy bit lines and energy recovery driver.

It shows energy saving of 37% compared to its conventional counterpart at 400 MHz/2.5V.

3. Adiabatic Register File

The register file stores data and provides the stored data to functional units. A 2-port ECRL register file is [7] shown (Fig. 6). The Efficient

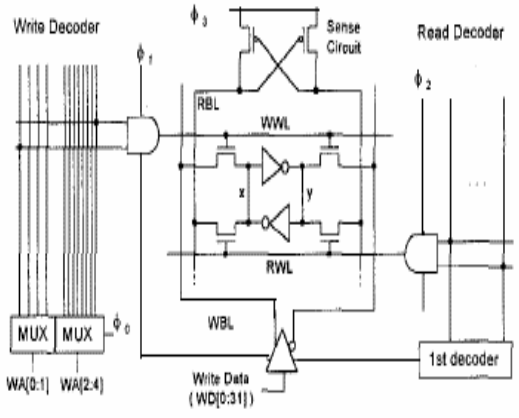

Fig. 6. ECRL register file.

Charge Recovery Logic (ECRL) uses 4-phase clock for correct operation and power saving. The ECRL register file consists of a storage cell, column/row decoder, sense amplifier and write circuit. All the circuits except the storage cell array are designed based on ECRL. The decoding block for selecting word line uses two-step decoding scheme. The 5-bit address is divided into 2 bits and 3 bits for decoding. Lowering the voltage of the write bit line carry out the write operation. A 32x32 ECRL register file shows energy saving of 72% compared to conventional CMOS register file.

A 2-read and 1-write multi-port reversible adiabatic logic, nRERL register file [8] is shown (Fig. 7). The nMOS reversible energy recovery logic

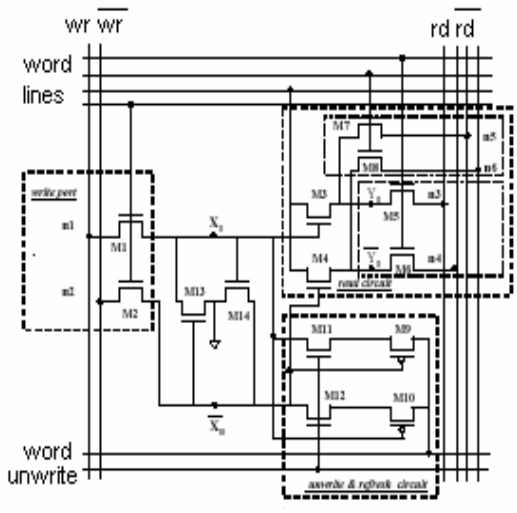

Fig. 7. nRERL register file.

(nRERL) uses a simpler 6-phase clocked power and bootstrapped nMOS switches. The nRERL register file discards garbage information with minimal energy dissipation. The storage cell consists of 14 transistors. It uses a 6-phase clock. This design with storage cell and other blocks are found to be advantageous only at low operating frequencies. A 16x8 nRERL register file shows energy saving of 93.4% compared to conventional register file at the frequency lower than 1 MHz.

4. Adiabatic CAM

The structure of a adiabatic CAM cell [9] is as shown (Fig. 8) except that the transistor N3 is connected to a clocked power supply (PC) instead of ground. The power clock causes adiabatic transitions in the match line thereby saving considerable energy.

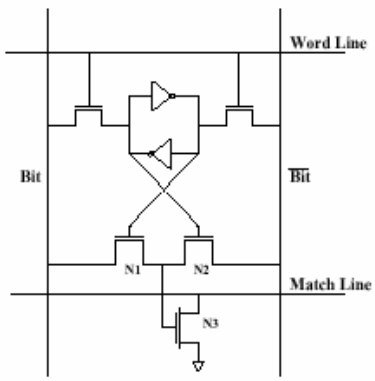

Fig. 8. Basic CAM cell.

Here the bit lines are pre-discharged and the search data is loaded onto the bit lines. The match line is pre-discharged initially. When a mismatch occurs, the transistor N3 is ON and the match line follows PC, thereby maintaining a very low potential drop across the match line capacitance. The swing in the match line is maintained to a value of one threshold voltage less than the full rail, to decrease the charge loss that would arise across the transistor N3. The charging and discharging path are the same for the match line and the charge stored is recovered in the same clock cycle. The match line is therefore held low after the evaluation phase, because the energy is recovered by ramping down the power clock.

When a match condition occurs the transistor N3 is OFF leaving the match line in a low state. This state causes no energy dissipation. For both conditions the energy dissipated is minimal and substantial energy saving is obtained. The output of this CAM is adiabatic and is valid when the power-clock is high. This adiabatic CAM [9] shows energy saving of 99.9% for 16x16 array when operated at 2 MHz. At 200 MHz the maximum frequency of operation, it shows energy savings of 20% and 45% for 16x16 and 32x32 CAM array respectively when compared with the basic CMOS CAM.

The Pass transistor Adiabatic Logic (PAL) CAM cell [10] is shown (Fig. 9). PAL an adiabatic logic family [11] is a dual-rail logic with true and complementary NMOS functional blocks and cross-coupled PMOS latch. A sinusoidal power clock (PC) supplies the PAL. The output will be valid only around the peak of the PC. When the PC ramps down towards zero the energy stored on the capacitance is recovered.

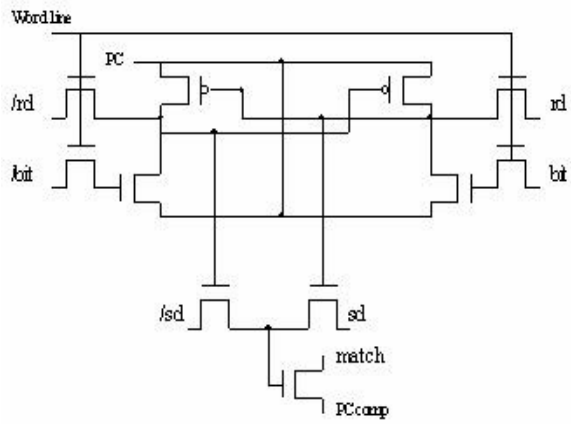

Fig. 9. PAL CAM cell.

The data lines (bit and /bit) are pre-charged by the PC to recover the energy before the write and the read operations. Separate data lines are used for writing and reading the data. In the compare operation, the charging and discharging path are made the same, which eliminates the need for pre-charging the match line. Whenever there is a hit, transistor connected to match line will be ON allowing the PCcomp to pass on the match line. If there is a miss, it will be OFFand the match line remains low. The PC and Pccomp may not be the same. It is sufficient that the PCcomp will have a value greater than the threshold voltage of the PMOS. The 16x16 array of the adiabatic CAM [10] shows energy saving of 95% at 10 MHz operating frequency compared to conventional CMOS design.

5. Conclusion

The work on adiabatic memories and its power reduction capabilities reported are listed out in this paper. Table 1 shows the percentage of energy savings of various adiabatic memories such as SRAM, register file and CAM when compared with the conventional CMOS counterpart. It is also found that low frequency, which is one of the major limitations of the adiabatic memories, has slowly overcome in the recent researches.

It also shows that further research on this area will bring out better result compared to the conventional schemes.

Table 1. Comparison of energy savings for several adiabatic memories

Memory type	Frequency [MHz]	% of energy savings
SRAM core in [2]	1	Around 85
256x256 SRAM in [3]	200	55
256x256 SRAM in [4]	300	62
128x256 fixed load SRAM in [5]	250	79
128x256 constant load SRAM in [6]	400	37
32x32 register file in [7]	200	72
16x8 nRERL register file in [8]	<1	93.4
32x32 CAM in [9]	200	45
16x16 PAL CAM in [10]	10	95

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