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SINGLE-ENDED FOUR-QUADRANT MULTIPLIER WITHOUT ANY PASSIVE COMPONENTS

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ABSTRACT

A CMOS four-quadrant analog multiplier has been designed without any passive components to produce a highly linear single-ended output. A fundamental Gilbert-cell circuit is coupled with a CMOS adder circuit and an operational amplifier to produce a highly linear four-quadrant multiplier. The circuit achieves high speed operation and eliminates all passive components. The entire circuit is designed using only CMOS. A symmetrical design approach is used to provide a self balanced output with higher accuracy, low offset and high linearity.

1. Introduction

One of the main issues in designing analog circuits is the requirement of passive components to realize a fully functional circuit. When using passive components in the circuits, there are parasitic elements associated with them. For example, while designing a passive resistor component using poly resist in CMOS or Bi-CMOS technology, there is a parasitic capacitance always associated with it. And for circuits such as amplifier circuits using opamps, higher value resistors are required to achieve the desired gain of the amplifier. But higher resistor values tend to reduce the speed and occupy more area. And most importantly, they are always associated with large parasitic capacitance. One of the techniques to eliminate problems due to parasitic capacitance is to replace passive resistors with active resistors. The design of an active resistor (voltage controlled resistor) can be found in [1–3]. But those circuits cannot be implemented in combination with other circuits such as an amplifier circuit using an operational amplifier. Because, active-resistor circuits explained in previous papers [1–3] can be operated only in two quadrants (quadrant I & III). However, using our novel design techniques, more accurate, faster and lower power circuits can be realized.

2. Methods

The fundamental equation of a closed loop system is given by Eq. 1.

$$A_c = \frac{A_0}{1 + \beta A_0} \tag{1}$$

where A_c is closed loop gain of the system, A_0 is open loop gain of the system, β is the feedback factor.

In a conventional operational amplifier circuit, the feedback circuit is designed by a resistor network (R_f and R_i). The ratio of the resistance value determines the feedback factor. However, implementing such a resistor network in VLSI circuits consumes a large amount of chip area and also introduces high parasitic capacitances. The parasitic capacitance ultimately lowers the operating frequency of the circuit. To avoid this problem, a new method in implementing an amplifier circuit without passive components along with a Gilbert-cell multiplier circuit is described. In this paper, a method to realize a four-quadrant analog multiplier circuit without passive components is explained in subsequent sections.

2.1. Four-quadrant multiplier

A four-quadrant Gilbert-cell multiplier circuit is coupled with a unity gain differential amplifier to realize a single-ended four-quadrant multiplier circuit. The schematic of a four-quadrant analog multiplier is shown in Fig. 1. Two cross-coupled current mode Gilbert-cells are used to realize the four-quadrant operation. The dimensions of all the transistors in the Gilbert-cell circuit are identical. A PMOS based Gilbert-cell is used in order to make

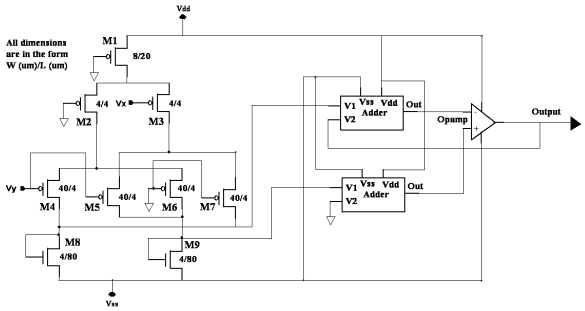

Fig. 1. Schematic diagram of four-quadrant multiplier with single-ended output.

the design compatible to an N-well process. Cross-coupled current outputs are converted into equivalent voltages using a diode connected NMOS load. The biasing circuit is a CMOS voltage divider circuit which utilizes PMOS operating at near threshold region. An important difference between this circuit and previously published four-quadrant multiplier circuits is the implementation of a unity gain differential amplifier to convert the differential output into a single-ended output. By this technique, a fully CMOS compatible multiplier circuit without passive components has been realized. More description about the methods to develop unity gain differential amplifiers is explained in Section 2.2. The dimensions of the transistors used in Gilbert-cell and its corresponding region of operation are presented in Table 1.

Table. 1. Summary of device dimension and its operating condition.

Device	Dimension W/L [μm/μm]	V_{ds} [V]	$V_{gs}-V_{th}$ [V]	Operating region
M1	8/20	0.78/0.87	1.6	Linear
M2	4/4	0.70/0.81	0.73/0.82	Saturation
M3	4/4	0.81/0.70	0.83/0.72	Saturation
M4	40/4	0.96/0.90	0.11/0.13	Near threshold
M5	40/4	0.84/1.02	0.13/0.11	Near threshold
M6	40/4	0.82/1.04	0.01/0.03	Near threshold
M7	40/4	0.98/0.87	0.03/0.01	Near threshold
M8	4/80	2.46/2.54	1.9/1.98	Saturation
M9	4/80	2.59/2.39	2.03/1.83	Saturation

2.2. Symmetric unity gain differential amplifier

In our current design, the large resistive network is replaced by active devices (using only CMOS logic) to implement the feedback network. In this design, a unity gain differential amplifier circuit is realized using a CMOS only adder circuit [4] in the feedback path.

The CMOS analog adder circuit explained in [4] has a disadvantage of systematic output offset voltage. To rectify and elaborate the function into a unity gain differential amplifier with low output offset voltage, a new configuration shown in Fig. 1 is used. The offset cancellation technique is described by Eq. (6). As explained in the Eq. (6), the use of two adders, one for each input, produces identical systematic-output offset voltages. This analysis ignores the effects of level-shifter output stage and mismatches in the output impedance of NMOS and PMOS [5] (assuming all the transistors of both the adder circuit are placed very close to each other in the ASIC to avoid mismatch in transistors during fabrication). A two stage operational amplifier is used to implement a high gain amplifier [5].

The voltage gain of the amplifier can be determined by the following equations:

$$V_{out} = (V_2 - (V_1 + V_{out}))A_0\,, \tag{2}$$

$$V_{out} = V_{in}A_0 + V_{out}A_0\,, \tag{3}$$

$$A_v = \frac{A_0}{1 - A_0}\,. \tag{4}$$

If $A_0 >> 1$ (ideally infinite) then

$$V_{out} = V_1 - V_2\,, \tag{5}$$

$$V_{out} + V_2 + V_{offset} = V_1 + V_{offset}\,. \tag{6}$$

This circuit is extremely helpful in converting a balanced differential signal to a single-ended output. Most of the circuits like the Gilbert-cell multipliers, differential amplifiers, opamps and current mode circuits can incorporate this topology to convert differential voltage signals or differential current signals into single-ended voltage signals. The same circuit shown in Fig. 1 can be used as an analog adder by interchanging one of its input terminals with the ground terminal. This circuit was designed and simulated using Cadence schematic capture in AMI-1.5 μm technology. The entire circuit was designed to be compatible with an N-well process. Hence, all the bulk terminals of NMOS transistors were tied to V_{ss} and all the bulk terminals of PMOS transistors were tied to their source terminals to make the body effect coefficient negligible.

3. Results

All the circuit mentioned above were simulated and tested using the HSpice simulation tool. Figure 2 depicts the simulation results of the CMOS only unity gain differential circuit. While sweeping one input voltage (V_1) from −100 mV to 100 mV, the other input voltage (V_2) was kept constant at three different values at −100 mV, 0, and 100 mV. Figure shows the output voltage swing from −200 mV to 0, −100 mV to 100 mV, 0 to 200 mV corresponding to input voltage (V_2) at −100 mV, 0, and 100 mV.

A four-quadrant multiplier circuit has been simulated and tested. Simulation results are depicted in Fig. 3. Two input voltages applied to the multiplier

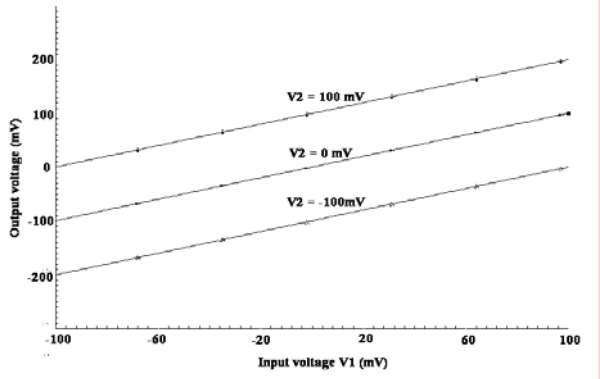

Fig. 2. Characteristics of unity gain differential amplifier.

circuits are V_x and V_y. Input voltage (V_x) was swept from −100 mV to 100 mV. And while sweeping V_x, V_y was kept constant at different values from −100 mV to 100 mV in steps of 20 mV. The output voltage was plotted by keeping input voltage (V_y) constant at −100 mV, −80 mV, −60 mV, −40 mV, −20 mV, 0, 20 mV, 40 mV, 60 mV, 80 mV, and 100 mV. The graph clearly shows the good linearity over the desired input and output voltage range.

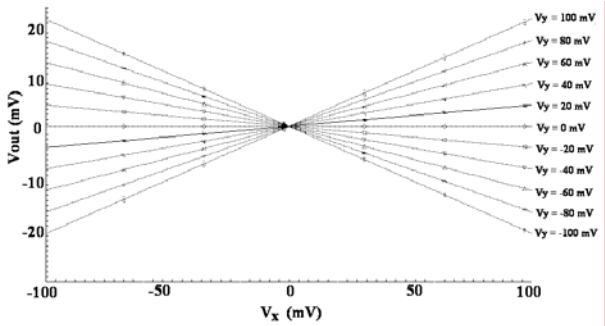

Fig. 3. Simulation output of four-quadrant multiplier.

The multiplier circuit was also characterized by applying two sine wave inputs. Zero degree phase difference was maintained between the input signals. Both the sine waves applied as input signals have amplitudes of 100 mV (−100 mV to 100 mV peak to peak). Figure 4 depicts the waveform obtained from

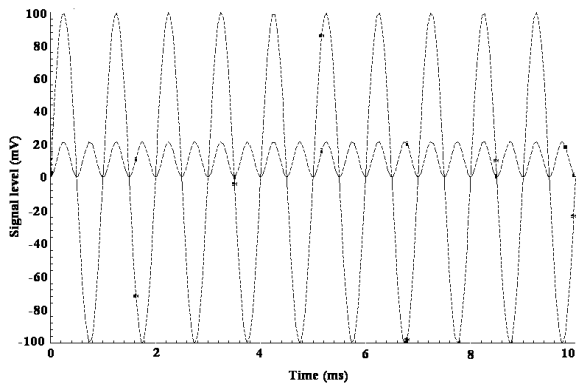

Fig. 4. Multiplier output for sin (θ_1) and sin (θ_2) as inputs (sin (θ_1)= = sin (θ_2))

the simulation of the four quadrant multiplier circuit. An output waveform of amplitude approximately 22 mV was obtained. As depicted in Fig. 4, the frequency of the output waveform is twice the frequency of the input waveform. A scaling amplifier can be added at the output to increase the output swing of the multiplier. In addition, a scaling amplifier at the input increases the input dynamic range.

To determine the level of harmonics present at the output, Fourier analysis of the transient waveform was done. The simulation output waveforms are shown in Fig. 5. A transient analysis of the multiplier

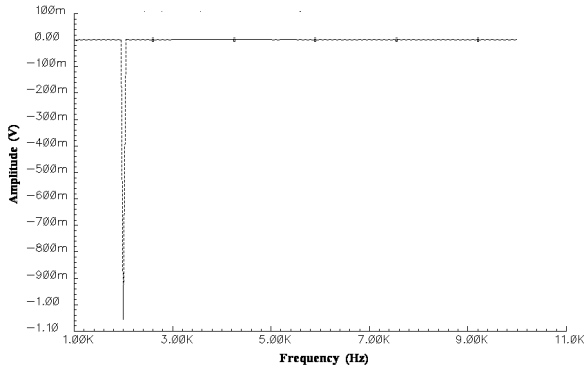

Fig. 5. Fourier analysis of the multiplier with 1 kHz input signal.

circuit was plotted first; later a Fourier transform of the resultant waveform was obtained. Data points were calculated at every 100 Hz and plotted against frequency. In this analysis, both the inputs are supplied with a 1 kHz sine wave signal of identical amplitudes and zero phase difference. A peak at 2 kHz can be seen from Fig. 5, showing the function of a frequency doubler circuit. Also, only negligible amounts of harmonics are present at the output.

4. Discussion

A single-ended four-quadrant multiplier circuit without any passive components was designed. Four-quadrant analog multiplier circuits using different circuit topologies have been reported [6–8]. However, to implement those circuits in a fully functional practical system, additional circuits are needed. For example, the most preferred form of output signal from an electrical circuit is a single-ended voltage output. One simple technique that is most widely used by today's circuit designer is a differential current mirror circuit. But, it has a drawback of non-zero output bias voltage.

An analog circuit in general requires a large number of passive components. A drawback of circuits with passive components is the presence of parasitic passive elements (parasitic capacitors, parasitic inductors and parasitic resistors) associated with them. For example, when a high value resistor is designed in poly-silicon in a CMOS technology, an unwanted parasitic capacitive element will be attached to it. This capacitance largely degrades the performance of the circuit. Also, designing resistive elements in a VLSI circuit occupies a large amount of chip area. This is one of the reasons that analog circuits are less popular as large scale integrated

circuits. The other important reason for non-usage of analog circuits in large scale integration is the high power dissipation. The later problem can be mitigated by having an additional power management circuit to avoid higher heat dissipation. Signal processing circuits in the analog domain consume considerably less energy [9]. The number of function implemented per area is far higher in the analog domain than in the digital domain. Hence, to implement any function in the analog domain, a design optimization can be followed to fine tune the power/area ratio. Analog circuits designed with dispersed circuit elements would lead to equivalent or lower power dissipation than the digital counterpart. As a result, the power dissipation per area can be reduced.

The main challenge is eliminating or minimizing the use of passive components in analog circuits. In this paper, realization of four-quadrant multiplier circuit without any passive components is achieved.

In the unity gain differential amplifier circuit, the feedback loop was designed using an analog adder circuit [4]. Symmetric design topology is utilized to avoid the systematic output voltage. The systematic offset voltage of the adders is cancelled by a symmetric design principle. Linear current to voltage converter circuits and linear voltage to current converter circuits are the main building blocks in realizing this circuit [10].

Unity gain differential amplifier (UGDA) is coupled with a Gilbert-cell multiplier circuit to realize a single-ended four-quadrant multiplier circuit. This can be easily integrated in any CMOS technology with the least space being occupied, resulting in a minimum area per function being achieved. The highly linear output resulting from such a circuit is shown in Fig. 4 and Fig. 5.

5. Conclusion

A single-ended four-quadrant multiplier has been successfully designed without any passive components. The circuit was simulated and tested. The multiplier designed has a low output offset voltage and high linearity and a higher speed of operation. This circuit was designed entirely to be compatible with any CMOS technology without any need for additional passive components.

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REFERENCES

1. N. TADIC, D. GOBOVIC, *A Voltage-Controlled Resistor in CMOS Technology Using Bisection of the Voltage Range*, IEEE Trans. on Instr. a. Measur., 2001, **50**, 1704–1710.
2. K. NAY, A. BUDAK: A *Voltage-Controlled Resistance with Wide Dynamic Range and Low Distortion*, IEEE Trans. on Circuits a. Systems, 1983, **30**, 770–772.
3. R. SENANI, *Realization of Linear Voltage-Controlled Resistance in Floating Form*, Electron. Lett., 1994, **30**, 1909–1911.
4. H. CHAOUI, *CMOS Analogue Adder*, Electron. Lett., 1995, **31**, 180–181.
5. D. A. JOHNS, M. KEN, *Analog Integrated Circuit Design*, John Wiley & Sons, 2002.
6. B. M. WILAMOWSKI: *VLSI Analog Multiplier/Divider Circuit*, IEEE ISIE, 1998, **2**, 493–496.
7. S. VLASSIS, S. SISKOS, *Analog CMOS Four-Quadrant Multiplier and Divider*, IEEE ISCAS, 1999, **5**, 383–386.
8. D. GHOSH, D. PATRANABIS, *A Simple Analog Divider Having Independent Control of Sensitivity and Design Conditions*, IEEE Trans. on Instr. a. Measur., 1990, **3**, 522–526.
9. G. E. R. COWAN, R. C. MELVILLE, Y. P. TISIVIDIS, *A VLSI Analog Computer/Digital Computer Accelerator*, IEEE J. of Solid-State Circuits, 2006, **41**, 42–53.
10. K. BULT, H. WALLINGA, *A Class of Analog CMOS Circuits Based on the Square-Law Characteristics of an MOS Transistor in Saturation*, IEEE J. of Solid-State Circuits, 1987, **3**, 357–365.